IXYS

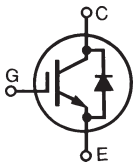
Preliminary Technical Information

# High Voltage, High Gain BiMOSFET™

**IXBK64N250**
**IXBX64N250**

$V_{CES}$ = 2500 V
$I_{C25}$ = 75 A
$V_{CE(sat)}$ ≤ 3.0 V

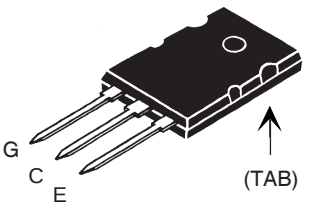
## Monolithic Bipolar MOS Transistor



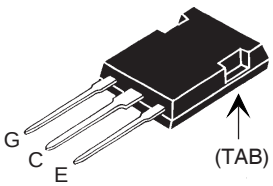

| Symbol | Test Conditions | Maximum Ratings | |
|---|---|---|---|
| $V_{CES}$ | $T_J$ = 25°C to 150°C | 2500 | V |
| $V_{GES}$ | Continuous | ±25 | V |
| $V_{GEM}$ | Transient | ±35 | V |
| $I_{C25}$ | $T_C$ = 25°C, Lead RMS limit | 75 | A |
| $I_{C110}$ | $T_C$ = 110°C | 64 | A |
| $I_{CM}$ | $T_C$ = 25°C, 1ms | 600 | A |
| **SSOA (RBSOA)** | $V_{GE}$ = 15V, $T_{VJ}$ = 125°C, $R_G$ = 3Ω<br>Clamped inductive load | $I_{CM}$ = 160<br>$V_{CES}$ = 2000 | A<br>V |
| $t_{SC}$ **(SCSOA)** | $V_{GE}$ = 15V, $T_J$ = 125°C,<br>$R_G$ = 5Ω, $V_{CE}$ = 1250V, non-repetitive | 10 | μs |
| $P_C$ | $T_C$ = 25°C | 735 | W |
| $T_J$ | | -55 ... +150 | °C |
| $T_{JM}$ | | 150 | °C |
| $T_{stg}$ | | -55 ... +150 | °C |
| $T_L$ | 1.6mm (0.063 in.) from case for 10s | 300 | °C |
| $T_{SOLD}$ | Plastic body for 10s | 260 | °C |
| $F_C$ | Mounting force (PLUS247™) | 20...120/4.5...27 | N/lb. |
| $M_d$ | Mounting torque (TO264) | 1.13/10 | Nm/lb.in. |
| **Weight** | (PLUS247™)<br>(TO-264) | 6<br>10 | g<br>g |

| Symbol | Test Conditions | | Characteristic Values ($T_J$ = 25°C, unless otherwise specified) Min. | Typ. | Max. | |
|---|---|---|---|---|---|---|
| $BV_{CES}$ | $I_C$ = 1mA, $V_{GE}$ = 0V | | 2500 | | | V |
| $V_{GE(th)}$ | $I_C$ = 4mA, $V_{CE}$ = $V_{GE}$ | | 3.0 | | 5.0 | V |
| $I_{CES}$ | $V_{CE}$ = 0.8$V_{CES}$<br>$V_{GE}$ = 0V | $T_J$ = 25°C<br>$T_J$ = 125°C | | | 50<br>6 | μA<br>mA |
| $I_{GES}$ | $V_{CE}$ = 0V, $V_{GE}$ = ±25V | | | | ±200 | nA |
| $V_{CE(sat)}$ | $I_C$ = $I_{C110}$, $V_{GE}$ = 15V | <br>$T_J$ = 125°C | | 2.5<br>3.1 | 3.0 | V<br>V |

**TO-264 (IXBK)**




**PLUS247™ (IXBX)**




G = Gate, C = Collector,
E = Emitter, TAB = Collector

### Features

- High Blocking Voltage
- International standard package
- Low conduction losses
- High current handling capability
- MOS Gate turn-on
  - drive simplicity

### Applications

- Uninterruptible power supplies (UPS)
- Switched-mode and resonant-mode power supplies
- Capacitor discharge circuits
- Laser Generators

### Advantages

- Easy to mount
- Space Savings
- High power density

| Symbol | Test Conditions ($T_J$ = 25°C, unless otherwise specified) | Characteristic Values Min. | Typ. | Max. | |
|---|---|---|---|---|---|
| $g_{fs}$ | $I_C$ = 64A, $V_{CE}$ = 10V, Pulse test, t ≤ 300µs, duty cycle ≤ 2 % | 40 | 72 | | S |
| $C_{ies}$ | $V_{CE}$ = 25V, $V_{GE}$ = 0V, f = 1MHz | | 10400 | | pF |
| $C_{oes}$ | | | 360 | | pF |
| $C_{res}$ | | | 120 | | pF |
| $Q_g$ | $I_C$ = 64A, $V_{GE}$ = 15V, $V_{CE}$ = 0.5 $V_{CES}$ | | 400 | | nC |
| $Q_{ge}$ | | | 46 | | nC |
| $Q_{gc}$ | | | 155 | | nC |
| $t_{d(on)}$ | **Resistive load, $T_J$ = 25°C** | | 49 | | ns |
| $t_{ri}$ | $I_C$ = 128A, $V_{GE}$ = 15V | | 318 | | ns |
| $t_{d(off)}$ | $V_{CE}$ = 1250V, $R_G$ = 1Ω | | 232 | | ns |
| $t_{fi}$ | | | 170 | | ns |
| $t_{d(on)}$ | **Resistive load, $T_J$ = 125°C** | | 54 | | ns |
| $t_{ri}$ | $I_C$ = 128A, $V_{GE}$ = 15V | | 578 | | ns |
| $t_{d(off)}$ | $V_{CE}$ = 1250V, $R_G$ = 1Ω | | 222 | | ns |
| $t_{fi}$ | | | 175 | | ns |
| $R_{thJC}$ | | | | 0.17 | °C/W |
| $R_{thCS}$ | | | 0.15 | | °C/W |

**Reverse Diode**

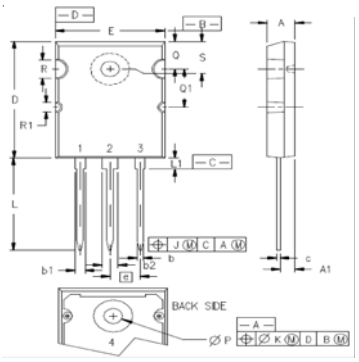
| Symbol | Test Conditions ($T_J$ = 25°C, unless otherwise specified) | Characteristic Values Min. | Typ. | Max. | |
|---|---|---|---|---|---|
| $V_F$ | $I_F$ = 64A, $V_{GE}$ = 0V, Pulse test, t ≤ 300 us, duty cycle, d ≤ 2% | | | 3.0 | V |
| $I_{RM}$ | $I_F$ = 64A, $V_{GE}$ = 0V, -$di_F/dt$ = 650A/µs | | 160 | | A |
| $t_{rr}$ | $v_R$ = 600V | | 480 | | ns |

Note:
Additional provisions for lead-to-lead isolation are required at $V_{CE}$ >1200V.

**PRELIMINARY TECHNICAL INFORMATION**

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

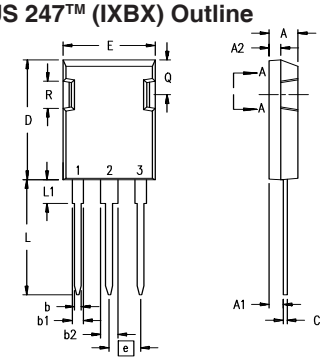
**TO-264 (IXBK) Outline**




1 – GATE
2, 4 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)

| SYM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | .185 | .209 | 4.70 | 5.31 |
| A1 | .102 | .118 | 2.59 | 3.00 |
| b | .037 | .055 | 0.94 | 1.40 |
| b1 | .087 | .102 | 2.21 | 2.59 |
| b2 | .110 | .126 | 2.79 | 3.20 |
| c | .017 | .029 | 0.43 | 0.74 |
| D | 1.007 | 1.047 | 25.58 | 26.59 |
| E | .760 | .799 | 19.30 | 20.29 |
| e | .215BSC | | 5.46 BSC | |
| J | .000 | .010 | 0.00 | 0.25 |
| K | .000 | .010 | 0.00 | 0.25 |
| L | .779 | .842 | 19.79 | 21.39 |
| L1 | .087 | .102 | 2.21 | 2.59 |
| ØP | .122 | .138 | 3.10 | 3.51 |
| Q | .240 | .256 | 6.10 | 6.50 |
| Q1 | .330 | .346 | 8.38 | 8.79 |
| ØR | .155 | .187 | 3.94 | 4.75 |
| ØR1 | .085 | .093 | 2.16 | 2.36 |
| S | .243 | .253 | 6.17 | 6.43 |

**PLUS 247™ (IXBX) Outline**



Terminals: 1 - Gate
2 - Drain (Collector)
3 - Source (Emitter)

| Dim. | Millimeter Min. | Millimeter Max. | Inches Min. | Inches Max. |
|---|---|---|---|---|
| A | 4.83 | 5.21 | .190 | .205 |
| $A_1$ | 2.29 | 2.54 | .090 | .100 |
| $A_2$ | 1.91 | 2.16 | .075 | .085 |
| b | 1.14 | 1.40 | .045 | .055 |
| $b_1$ | 1.91 | 2.13 | .075 | .084 |
| $b_2$ | 2.92 | 3.12 | .115 | .123 |
| C | 0.61 | 0.80 | .024 | .031 |
| D | 20.80 | 21.34 | .819 | .840 |
| E | 15.75 | 16.13 | .620 | .635 |
| e | 5.45 BSC | | .215 BSC | |
| L | 19.81 | 20.32 | .780 | .800 |
| L1 | 3.81 | 4.32 | .150 | .170 |
| Q | 5.59 | 6.20 | .220 | 0.244 |
| R | 4.32 | 4.83 | .170 | .190 |

**Fig. 1. Output Characteristics @ 25ºC**

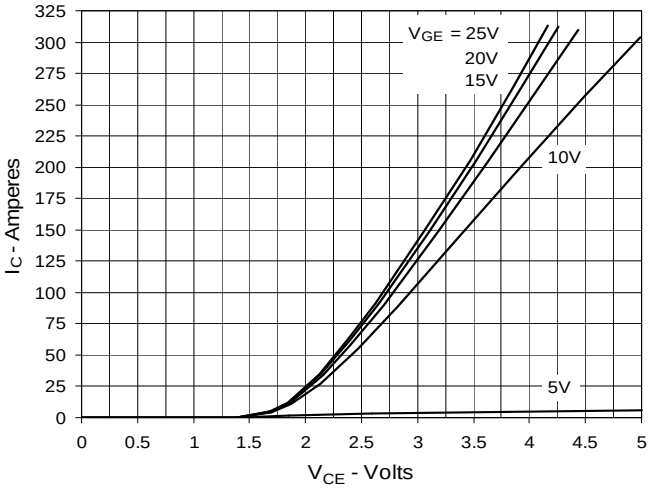



**Fig. 2. Output Characteristics @ 125ºC**

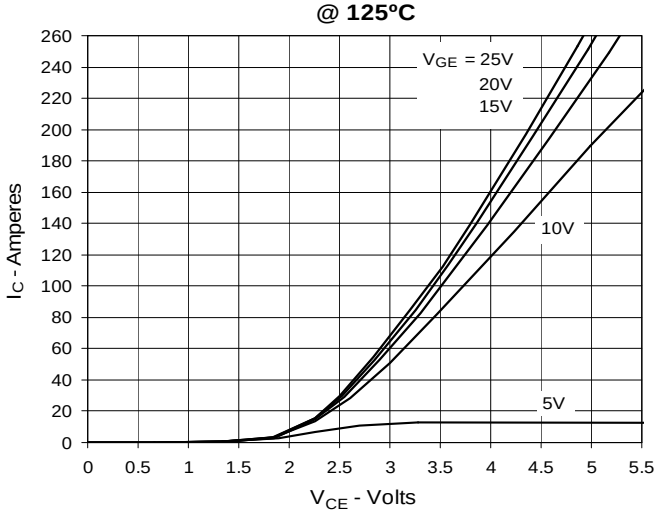



**Fig. 3. Dependence of $V_{CE(sat)}$ on Junction Temperature**

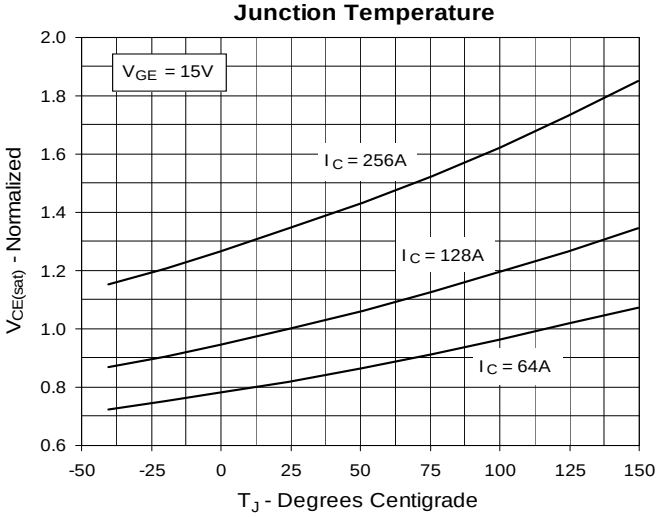



**Fig. 4. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage**

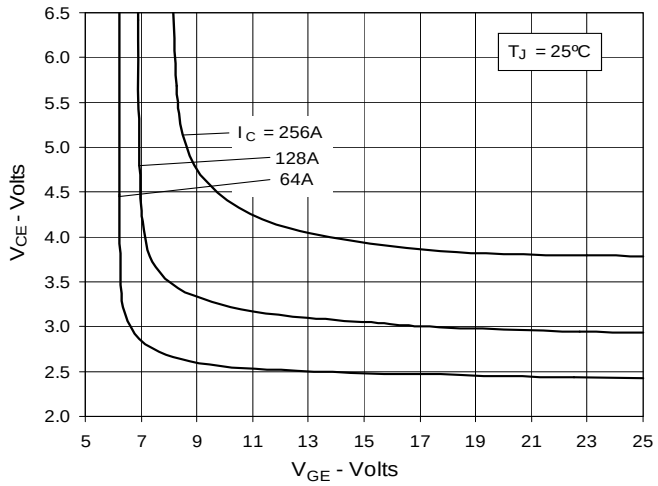



**Fig. 5. Breakdown & Threshold Voltages vs. Junction Temperature**

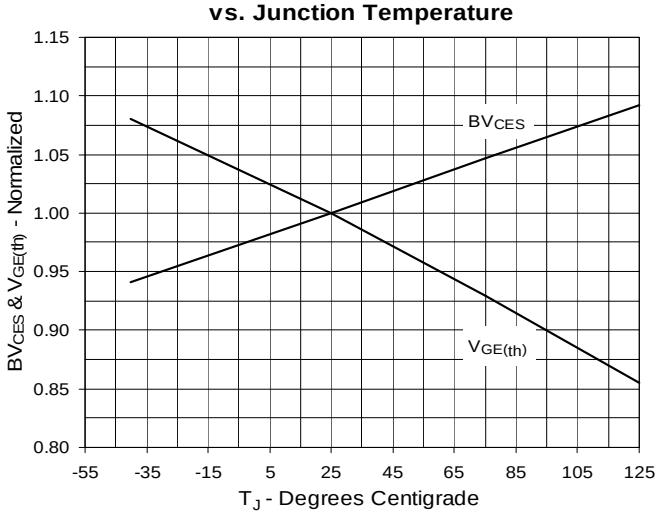



**Fig. 6. Input Admittance**

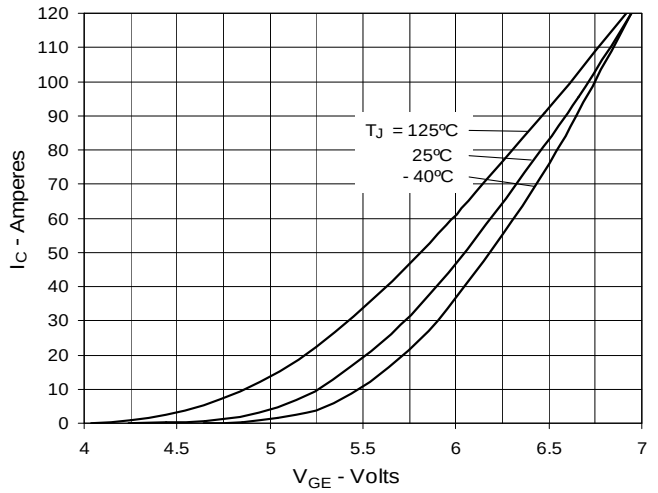


**Fig. 7. Transconductance**

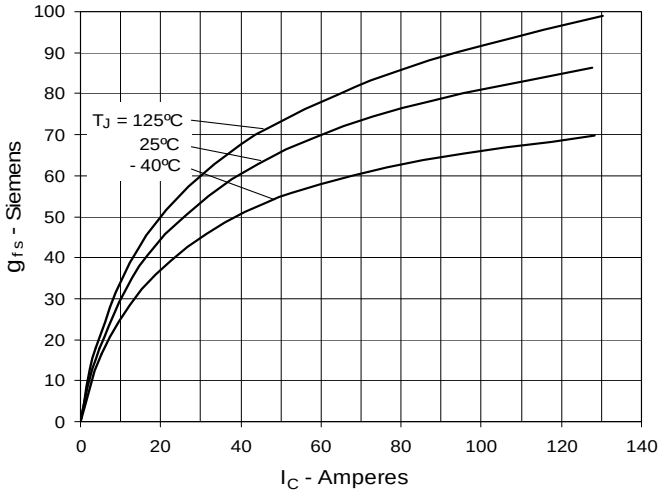



**Fig. 8. Forward Voltage Drop of Intrinsic Diode**

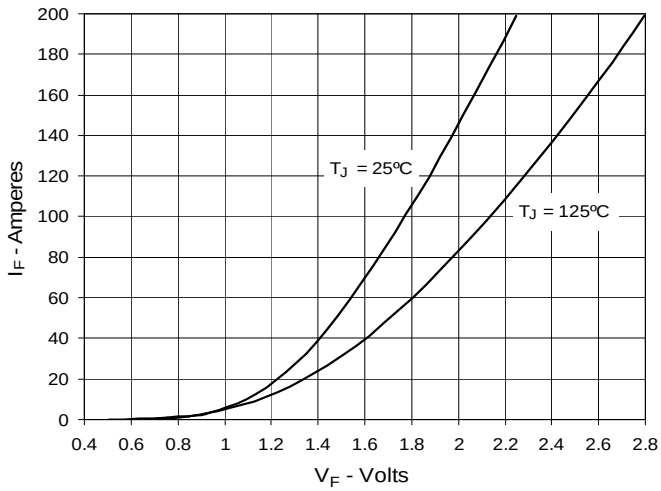



**Fig. 9. Gate Charge**

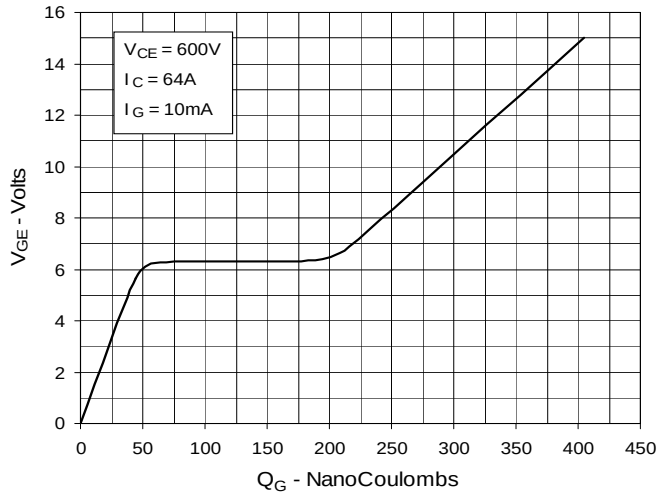



**Fig. 10. Capacitance**

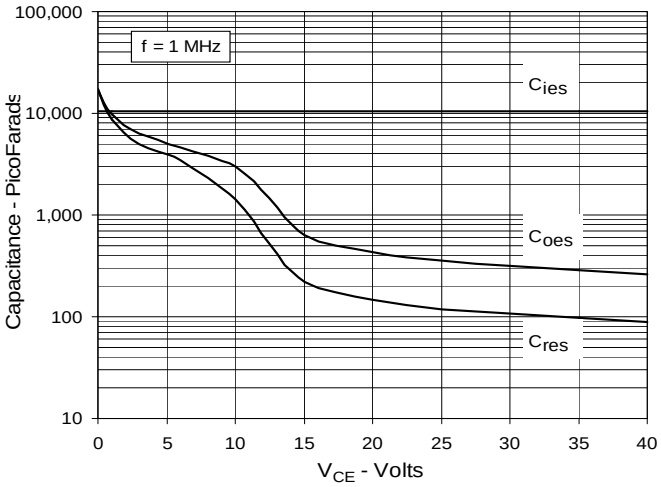



**Fig. 11. Reverse-Bias Safe Operating Area**

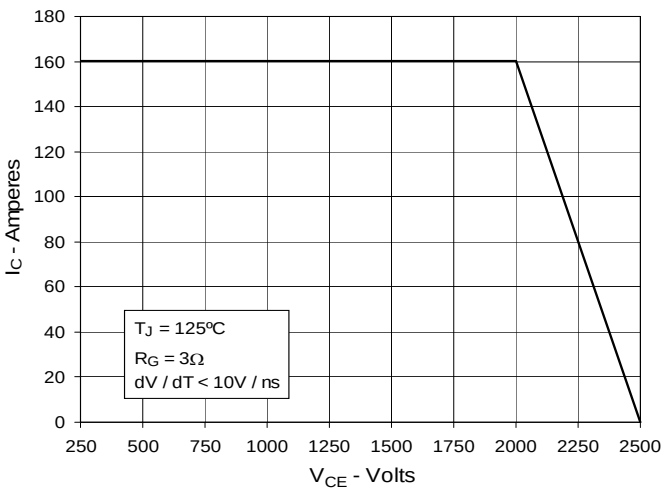



**Fig. 12. Maximum Transient Thermal Impedance**

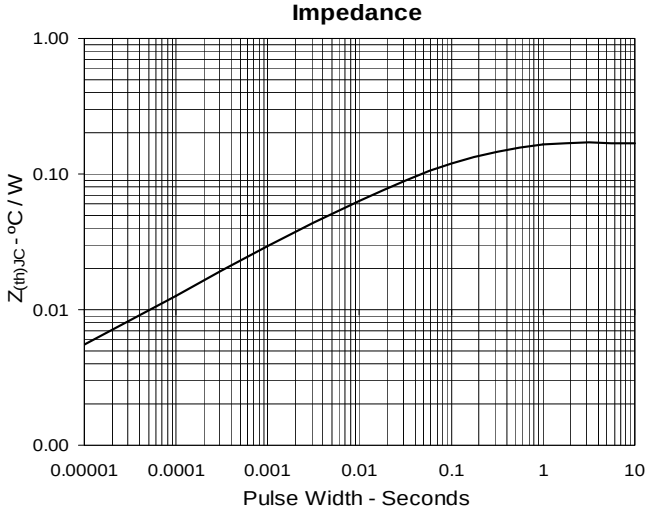


**Fig. 13. Resistive Turn-on Rise Time vs. Junction Temperature**

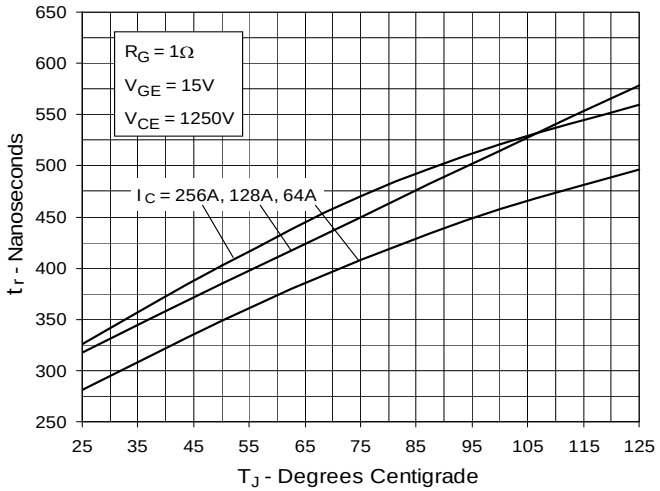



**Fig. 14. Resistive Turn-on Rise Time vs. Drain Current**

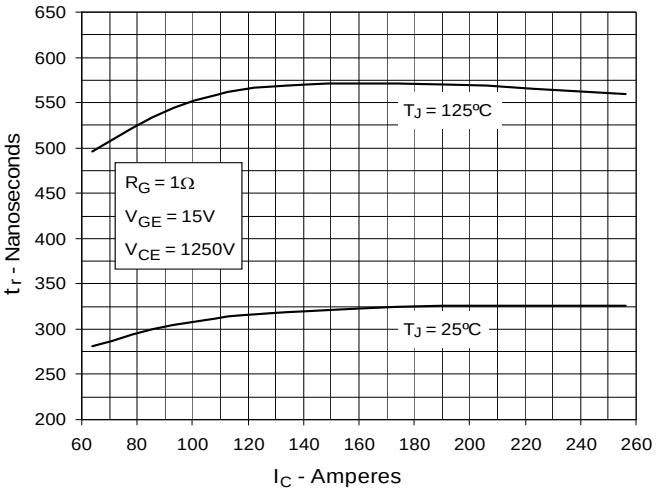



**Fig. 15. Resistive Turn-on Switching Times vs. Gate Resistance**

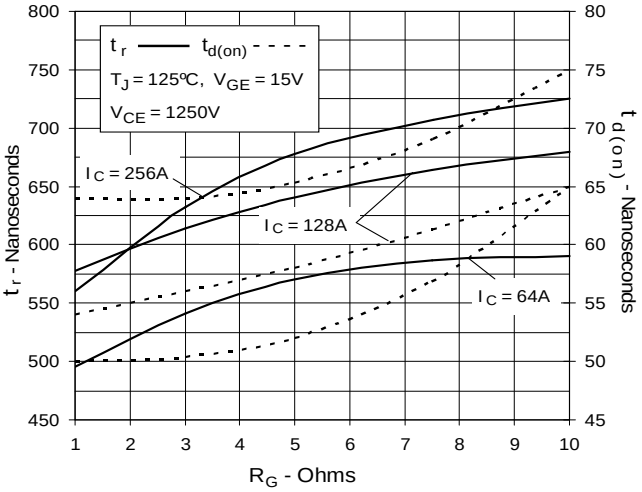



**Fig. 16. Resistive Turn-off Switching Times vs. Junction Temperature**

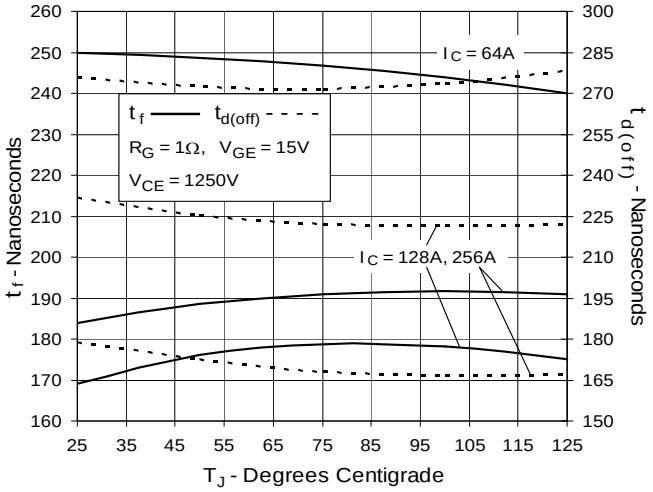



**Fig. 17. Resistive Turn-off Switching Times vs. Drain Current**

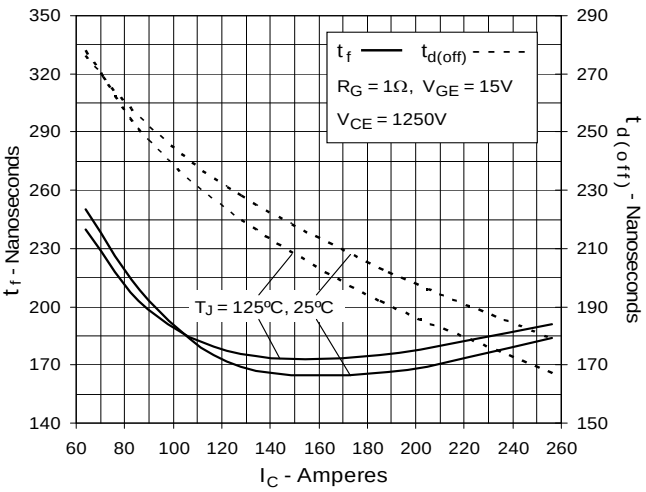



**Fig. 18. Resistive Turn-off Switching Times vs. Gate Resistance**